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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,569	11/06/2001	Hajime Kimura	SEL 288	8170

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EXAMINER	
JORGENSEN, LELAND R	
ART UNIT	**PAPER NUMBER**
2675	3

DATE MAILED: 01/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,569	KIMURA, HAJIME	
	Examiner	Art Unit	
	Leland R. Jorgensen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 101* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 101* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 November 2001* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 4/2
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the supply and drains for each TFT described in claims 1 - 101 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 21, 23, 26, 28, 31, 33, 84, 86, 89, 91, 94, 96, 99, and 101 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 21, 23, 26, 28, 31, 33, 84, 86, 89, 91, 94, 96, 99, and 101 recites the limitation "the first current controlling element." There is insufficient antecedent basis for this limitation in the claim. Note also that claim 101 is incomplete.

Double Patenting

4. Applicant is advised that should claims 21, 26, 31, 84, 89, or 94 be found allowable, claims 23, 28, 33, 86, 91, or 96 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 3 - 7, 16, 18, 20, 22, 24, 30, 32, 34 – 50, 83, 85, 87, 93, 95, and 97 are rejected under 35 U.S.C. 102(e) as being anticipated by Dawson et al., USPN 6,229,506 B1.

Claims 1, 16, 18

Dawson teaches a light emitting device comprising a plurality of pixels. Dawson, col. 6, lines 56 – 60; and figure 5. Each of the plurality of pixels [pixel structure 200] comprises an EL driving TFT [PMOS transistor 260 (P2)]; an electric discharge TFT [PMOS transistor 250 (P1)]; an EL element [OLED 290] ; and a reference power supply line [Data line 220]. Dawson, col. 3, lines 11 – 22; and figure 2. A source region of the EL driving TFT is connected to the power

supply line [V_{DD} 295 through NMOS transistor 270 (N1)] and a drain region of the EL driving TFT is connected to a pixel electrode of the EL element. Dawson, col. 3, lines 11 – 22; and figure 2. A drain region of the electric discharge TFT is connected to the power supply line [through NMOS transistor 270 (N1)] and a source region of the electric discharge TFT is connected to the reference power supply line. Dawson, col. 3, lines 11 – 22; and figure 2.

Claim 3

Dawson teaches a light emitting device comprising a plurality of pixels. Dawson, col. 6, lines 56 – 60; and figure 5. Each of the plurality of pixels [pixel structure 200] comprises an EL driving TFT [PMOS transistor 260 (P2)]; an electric discharge TFT [PMOS transistor 250 (P1)]; an EL element [OLED 290] ; and a reference power supply line [Data line 220]. Dawson, col. 3, lines 11 – 22; and figure 2. Dawson teaches that the EL driving TFT controls the amount of a current supplied from the power supply line the to the EL element, and the electric discharge TFT controls the amount of a current supplied from the power supply line to the reference power supply line when the EL driving TFT is turned OFF. Dawson, col. 3, lines 22 – 54.

Claims 4 - 7

Dawson teaches a light emitting device comprising a plurality of pixels. Dawson, col. 6, lines 56 – 60; and figure 5. Each of the plurality of pixels [pixel structure 200] comprises an EL driving TFT [PMOS transistor 260 (P2)]; an electric discharge TFT [PMOS transistor 250 (P1)]; an EL element [OLED 290] ; and a reference power supply line [Data line 220]. Dawson, col. 3, lines 11 – 22; and figure 2. A source region of the EL driving TFT is connected to the power supply line [V_{DD} 295 through NMOS transistor 270 (N1)] and a drain region of the EL driving TFT is connected to a pixel electrode of the EL element. Dawson, col. 3, lines 11 – 22; and

figure 2. A drain region of the electric discharge TFT is connected to the power supply line [through NMOS transistor 270 (N1)]. Dawson, col. 3, lines 11 – 22; and figure 2.

Dawson teaches that a predetermined electric potential [through constant current source 230] is applied to a source region of each of the plurality of electric discharge TFTs. Dawson, col. 3, lines 32 – 53. A current flows through a channel formation region of each of the plurality of electric discharge TFTs when each of the plurality of EL elements does not emit light. Dawson, col. 3, line 55 – col. 4, line 5. Each of the plurality of electric discharge TFTs is turned OFF when each the plurality of EL elements emits light. Dawson, col. 3, line 32 – col. 4, line 5. A current flows through a channel formation region of each of the plurality of EL driving TFTs when each of the plurality of EL elements emits light. Dawson, col. 3, lines 32 – 53.

Claims 20, 30, 83, 93

Dawson teaches that the source region of the electric discharge TFT [PMOS transistor 250 (P1)] is connected to a first current controlling element [current source 230], and that the source region of the electric discharge TFT [PMOS transistor 260 (P2)] receives a given electric potential through the first current controlling element. Dawson, col. 3, lines 32 – 53; and figure 2.

Claims 22, 32, 85, 95

Dawson teaches that drain region of the electric discharge TFT [PMOS transistor 250 (P1)] is connected to the power supply line through a second current controlling element [NMOS transistor 270 (N1)]. Dawson, col. 3, lines 11 – 22; and figure 2.

Claims 24, 34, 38, 42, 46, 50, 87, 97

Dawson teaches that an electronic device that comprises the light emitting device. Dawson, col. 7, lines 7 – 13.

Claims 35, 39, 43, 47

Dawson teaches that switching of the plurality of EL driving TFTs and the plurality of electric discharge TFTs is controlled by digital video signals inputted to the gate electrodes of the plurality of EL driving TFTs and the gate electrodes of the plurality of electric discharge TFTs. Dawson, col. 3, lines 11 – 22; and figure 2.

Claims 36, 40, 44, 48

Dawson teaches that the digital video signals are inputted to the gate electrodes of the plurality of EL driving TFTs and the gate electrodes of the plurality of electric discharge TFTs through respective switching TFTs. Dawson, col. 3, lines 11 – 22; and figure 2.

Claims 37, 41, 45, 49

Dawson teaches that the switching TFTs and the electric discharge TFTs have the same polarity. Dawson, col. 3, lines 11 – 22; and figure 2.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 2, 8 - 17, 19, 51, 55, 59, 63, 67, 71, 75, and 79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemura, USPN 5,576,857 in view of Sano, USPN 6,628,363 B1.

Claims 1, 2, 16, 17, 19

Takemura teaches a light emitting device comprising a plurality of pixels connected to a power supply line [column line Y_m]. Each of the plurality of pixels comprises an EL driving TFT (PMOS FET); an electric discharge TFT (NMO FETS); a pixel $Z_{n,m}$, and a reference power supply line [row lines X_n]. Takemura, col. 1, lines 14 – 20; col. 6, lines 14 – 36; and figure 6(B). A source region of the EL driving TFT is connected to the power supply line and a drain region of the EL driving TFT is connected to a pixel electrode. A drain region of the electric discharge TFT is connected to the power supply line and a source region of the electric discharge TFT is connected to the reference power supply line. A gate electrode of the EL driving TFT is connected to a gate electrode of the electric discharge TFT. Takemura, col. 6, lines 24 – 36; and figure 6(B). The polarity of the EL driving TFT (being a PMOS) is different from the polarity of the electric discharge TFT (being a NMOS).

Although Takemura teaches that the pixel electrode is for a LCD pixel, Takemura adds,

> The present invention is also applied to other type displays capable of forming grayscale images in accordance with customary analog grading systems or digital grading systems as proposed by the applicants, e.g. as described in Japanese Application No. Hei 3-163873.

Takemura, col. 14, lines 51 – 55. Takemura, however, does not specifically teach that the pixel has a EL element.

Sano teaches that a TFT active matrix can be used to drive both LDC and EL pixels. Sano, col. 1, lines 14 – 19.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the light emitting TFT circuit as taught by Takemura to drive EL pixels as taught by Sano as TFT circuits for EL devices as nearly the same as TFT circuits for LCD devices. Sano teaches such similarities.

> In a flat display such as a liquid crystal display or an organic electroluminescence (EL) display, arrangement is such that switching elements (thin film transistors) of the display part and a drive circuit for driving the switching elements are formed on the same substrate.

Sano, col. 4, lines 19 – 23. Sano adds,

> In the process for building the display, formation of the thin film transistors precedes rubbing on the planarization insulating film and enclosure of liquid crystal material in the case of the liquid crystal display or the formation of the EL element part in the case of the organic EL display, all of which may increase the possibility allowing the invasion of impurity ions causing accumulation of electric charge.

Sano, col. 4, lines 41 – 47. Sano concludes,

> Furthermore, in the above embodiments, description has been given of the example employing a configuration in which the source electrode overlaps the TFT channel region, as the configuration of the thin-film transistor of the drive circuit, in particular, of the thin film transistor of the drive circuit formed on the same substrate as the LCD display. However, the present invention is not limited to this, and the above TFT structure is otherwise applicable to the configuration of the drive circuit of the organic EL display or the like (see FIG. 12). More specifically, the above configuration in which the source electrode overlaps the channel is applicable to the drive circuit for driving the organic EL display part, in particular, to the drive circuit which is formed on the same substrate as that display. Such a configuration makes it possible to prevent any variation in characteristic of the thin-film transistor in the drive circuit in the same manner as the case of the LCD.

Sano, col. 10, lines 9 – 25.

Claims 8 - 15

Takemura teaches a light emitting device comprising a plurality of pixels connected to a power supply line [column line Y_m]. Each of the plurality of pixels comprises an EL driving TFT (PMOS FET); an electric discharge TFT (NMO FETS); a pixel $Z_{n,m}$, and a reference power supply line [row lines X_n]. Takemura, col. 1, lines 14 – 20; col. 6, lines 14 – 36; and figure 6(B). A source region of the EL driving TFT is connected to the power supply line and a drain region of the EL driving TFT is connected to a pixel electrode. A drain region of the electric discharge TFT is connected to the power supply line and a source region of the electric discharge TFT is connected to the reference power supply line. A gate electrode of the EL driving TFT is connected to a gate electrode of the electric discharge TFT. Takemura, col. 6, lines 24 – 36; and figure 6(B). The polarity of the EL driving TFT (being a PMOS) is different from the polarity of the electric discharge TFT (being a NMOS). Takemura teaches that a predetermined electric potential is applied to a source region of each of the plurality of electric discharge TFTs, that a current flows through a channel formation region of each of the plurality of electric discharge TFTs when each of the plurality of EL elements does not emit light, and that each of the plurality of electric discharge TFTs is turned OFF when each the plurality of EL elements emits light. Takemura, col. 4, lines 48 – 63; col. 6, line 14 – col. 7, lines 46.

Although Takemura teaches that the pixel electrode is for a LCD pixel, Takemura adds, "The present invention is also applied to other type displays capable of forming grayscale images in accordance with customary analog grading systems or digital grading systems..." Takemura, col. 14, lines 51 – 55. Takemura, however, does not specifically teach that the pixel has a EL element.

Sano teaches that a TFT active matrix can be used to drive both LDC and EL pixels. Sano, col. 1, lines 14 – 19.

For the reasons stated in the rejection of claims 1, 2, 16, and 17 above, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the light emitting TFT circuit as taught by Takemura to drive EL pixels as taught by Sano as TFT circuits for EL devices as nearly the same as TFT circuits for LCD devices.

Claims 51, 55, 59, 63, 67, 71, 75, 79

Takemura teaches that the switching of the plurality of EL driving TFTs and the plurality of electric discharge TFTs is controlled by digital video signals inputted to the gate electrodes of the plurality of EL driving TFTs and the gate electrodes of the plurality of electric discharge TFTs. Takemura, col. 6, line 14 – col. 7, line 46.

9. Claims 25, 27, 29, 52 – 54, 56 – 58, 60 – 62, 64 – 66, 68 – 70, 72 – 74, 76 – 78, 80 – 82, 88, 90, 92, 98, and 100 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemura in view of Sano as applied to claims 2 or 17 above, and further in view of Dawson.

Claims 25, 88, 98

Neither Takemura nor Sano specifically teach a first current controlling element.

Dawson teaches that the source region of the electric discharge TFT [PMOS transistor 250 (P1)] is connected to a first current controlling element [current source 230], and that the source region of the electric discharge TFT [PMOS transistor 260 (P2)] receives a given electric potential through the first current controlling element. Dawson, col. 3, lines 32 – 53; and figure 2.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the first controlling element as taught by Dawson with the light emitting device as taught by Takemura and Sano to produce a constant current source. Dawson invites such combination by teaching,

> However, it has been observed that the brightness of the OLED is proportional to the current passing through the OLED. Therefore, a need exists in the art for a pixel structure and concomitant method that reduces current nonuniformities and threshold voltage variations in a "drive transistor" of the pixel structure.

Dawson, col. 2, lines 4 – 9. Dawson adds,

> In one embodiment of the present invention, a current source is incorporated in a LED (OLED) pixel structure that reduces current nonuniformities and threshold voltage variations in a "drive transistor" of the pixel structure. The current source is coupled to the data line, where a constant current is initially programmed and then captured.
>
> In another embodiment, the constant current is achieved by initially applying a reference voltage in an auto-zero phase that determines and stores an auto zero voltage. The auto zero voltage effectively accounts for the threshold voltage of the drive transistor. Next, a data voltage which is referenced to the same reference voltage is now applied to illuminate the pixel.

Dawson, col. 2, lines 13 – 25. Dawson specifically adds that it could be applied to a circuit where NMOS is used instead of PMOS as shown in Dawson, figure 2. Dawson states,

> Although the present invention is described using PMOS transistors, it should be understood that the present invention can be implemented using NMOS transistors, where the relevant voltages are reversed. Namely, the OLED is now coupled to the source of the NMOS drive transistor. By flipping the OLED, the cathode of the OLED should be made with a transparent material.

Dawson, col. 7, lines 13 – 19.

Claims 27, 90, 100

Dawson teaches that drain region of the electric discharge TFT [PMOS transistor 250 (P1)] is connected to the power supply line through a second current controlling element [NMOS transistor 270 (N1)]. Dawson, col. 3, lines 11 – 22; and figure 2.

Claims 52, 56, 60, 64, 68, 72, 76, 80

Dawson teaches that the digital video signals are inputted to the gate electrodes of the plurality of EL driving TFTs and the gate electrodes of the plurality of electric discharge TFTs through respective switching TFTs. Dawson, col. 3, lines 11 – 22; and figure 2.

Claims 53, 57, 61, 65, 69, 73, 77, 81

Dawson teaches that the switching TFTs and the electric discharge TFTs have the same polarity. Dawson, col. 3, lines 11 – 22; and figure 2.

Claims 29, 54, 58, 62, 66, 70, 74, 78, 82, 92

Dawson teaches that an electronic device that comprises the light emitting device. Dawson, col. 7, lines 7 – 13.

10. Claims 21, 23, 26, 28, 31, 33, 84, 86, 89, 91, 94, 96, 99, and 101 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson in view of Sedra and Smith, *Microelectronic Circuits*, 3rd ed. (New York; Saunders College Publishing, 1991) pp. 462 – 466, or unpatentable over Takemura in view of Sano and Dawson et al. as applied to claims 2 or 17 above, and further in view of Sedra and Smith.

Claims 21, 23, 26, 28, 31, 33, 84, 86, 89, 91, 94, 96, 99, and 101

Neither Takemura, Sano, nor Dawson teach that the first current controlling element is one of a resistor, a diode, and a TFT.

Sedra and Smith teach a current controlling element that is one of a resistor [output resistance R_O], a diode [D1 or D2], and a TFT [Q1 – Q3]. Sedra and Smith, pp. 462 – 466; and figure 6.41.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the current controlling element of Sedra and Smith with the light emitting device of Dawson or of Takemura, Sano, and Dawson to increase the output resistance of the current source to create a constant current source.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yamazaki et al., USPN 5,888,858; and Sasaki, USPN 5,818,068, each teach the use of same TFT circuits for both EL or LCD displays.

Bae, USPN 6,570, 338 B2; Kim, USPN 6,535,185 B2; Kawashima et al., USPN 6,091,203; and Yanai et al. USPN 6,011,532, each teach a display having back to back TFTs.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland Jorgensen whose telephone number is 703-305-2650. The examiner can normally be reached on Monday through Friday, 7:00 a.m. through 3:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven J. Saras can be reached on 703-305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, telephone number (703) 306-0377.

lrj

STEVEN SARAS
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